

Next-Generation Virtuoso Platform: Welcome to the New Sound of Analog Design

EMBARGOED UNTIL APRIL 5th (7:45 AM PST)

cādence®

What are we announcing?

Cadence® Virtuoso® ADE Product Suite

- Virtuoso ADE Explorer
 - Built for performance to get the analog circuit up and running in the initial stages of the design cycle
- Virtuoso ADE Assembler
 - Built for handling numerous acceptance tests for the design under various environmental conditions
- Virtuoso Variation Option
 - Built to assure accurate variation analysis is done for advanced nodes and high-yield products
- Virtuoso ADE Verifier
 - Built to provide electrical verification compliance status for all of the analog blocks being designed and coalesced into a single design

*These tools work in parallel with our existing
Virtuoso Analog Design Environment L, XL, and GXL
suite of tools*



The Analog Verification Problem: What's Needed Across Different Industries?

Let's look at verification for functional safety

Automotive

- Traceability
- Specification linkage
- Change management
- Reproducible results

Requirement-driven
SoC verification

- Fault injection
- Fault simulation
- Multiple abstractions
- Safety reports

Verification for
functional safety (ASIL)

ISO 26262



Medical devices are highly regulated

A failure here could mean life or death

- 1 general standard
- 10 collateral standards
- 60 particular standards
- Traceability is key to each

Set of applicable standards

- Package integrity tests
- Failure modes and effects analysis
- Thermal analysis
- Worst-case analysis

Examples of FDA demanded verification methods*

*FDA: *Design Control Guidance For Medical Device Manufacturers*
** 60601 Medical Electronics and 62304 Software contained within

IEC 60601**

IEC 62304**



Government Regulatory Agencies

FDA:	United States
EMA:	Europe
PMDA:	Japan
CFDA:	China
CDSCO:	India

IoT

Security verification is unfolding



“Police Body Cams Pre-Installed with Notorious Conficker Worm.”

“One of the world’s most notorious pieces of malware is found on body cams from Martel.”

Source: arstechnica
11/16/15



“Kids using ‘Hello Barbie’ won’t only be talking to a doll, they’ll be talking directly to a toy conglomerate whose only interest in them is financial. It’s creepy – and creates a host of dangers for children and families.”

Source: commercialfreechildhood.org
12/15/15



“The Terrifying Search Engine That Finds Internet-Connected Cameras, Traffic...”

Source: Forbes
9/23/2013

U.S. SENATE COMMITTEE ON
COMMERCE, SCIENCE, & TRANSPORTATION
SENATOR JOHN THUNE, CHAIRMAN • SENATOR BILL NELSON, RANKING MEMBER

HEARINGS

HOME / HEARINGS

February 11, 2015

The Connected World: Examining the Internet of Things
253 Russel Senate Office Building

 **FEDERAL TRADE COMMISSION**
PROTECTING AMERICA'S CONSUMERS

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ABOUT THE FTC NEWS & EVENTS ENFORCEMENT POLICY TIPS & ADVICE

News & Events » Press Releases » FTC Report on Internet of Things Urges Companies to Adopt Best Practices to Address Security Risks

FTC Report on Internet of Things Urges Companies to Adopt Best Practices to Address Consumer Privacy and Security Risks

Report Recognizes Rapid Growth of Connected Devices Offers Societal Benefits, But Also Risks That Could Undermine Consumer Confidence

FOR RELEASE
January 27, 2015

Source: <http://www.ftc.gov>

Customers need to make analog/mixed-signal verification *traceable*



Medical
IEC 62304
2006

FDA: *Design Control Guidance For Medical Device Manufacturers*

The results of the design verification, including identification of the design, method(s), the date, and the individual(s) performing the verification, shall be documented in the Design History File.



Aviation
DO-254
2006

In the consumer industry, “first-time right” is key and failures of a large mixed-signal chip due to analog problems are no longer acceptable.



Automotive
ISO 26262
2012

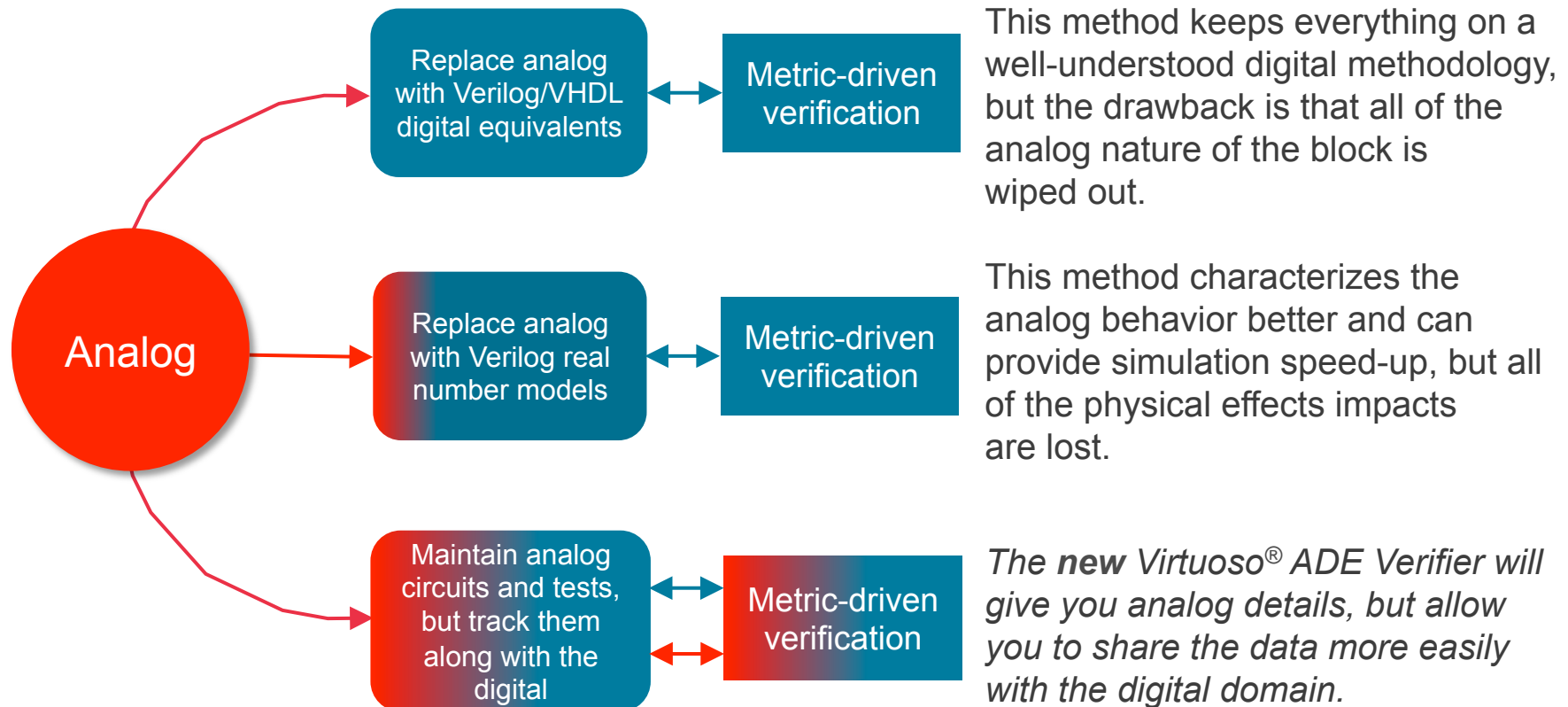
The challenge is, how do you make the analog design traceable?




Industrial
IEC 61508
1998

Crossing the verification chasm

When it comes to mixed-signal, it is all about choices





What is Cadence doing about analog mixed-signal verification?

Analog design traceability

How is it done today?

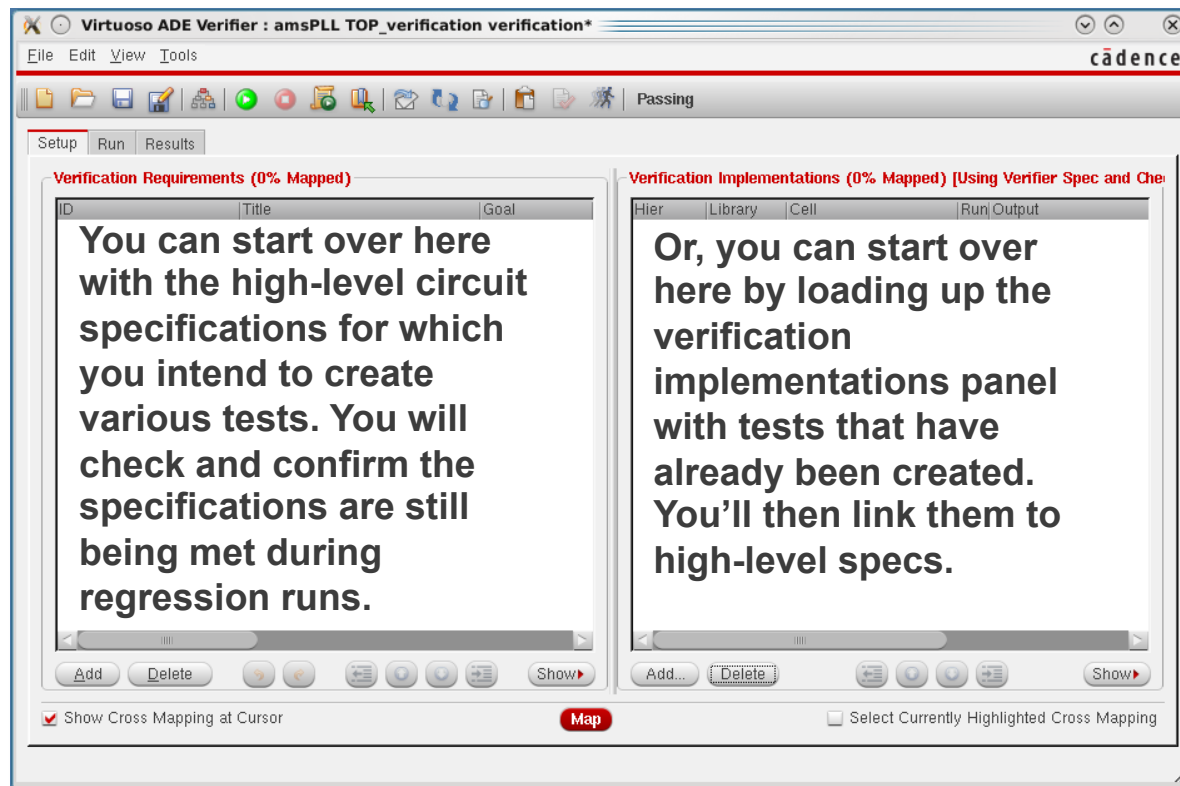
- Lots of manual intervention to determine the state of “verification” for each block
 - Use of spreadsheets is prevalent, but they are disconnected from the software and, therefore, updates are easily missed
- Convert the analog to digital and use the standardized digital, metric-driven flows, hoping that the physical implementations don’t disrupt signal quality too much
- Sometimes homegrown solutions are built by CAD teams since EDA vendors hadn’t provided this capability to the analog world before

What Cadence provides in the next-gen Virtuoso platform



Verification Engineer/Project Lead

- Able to run 100s of complex, interdependent simulations
- Monitor job status with complete control over simulator queuing
- Get a quick overview of the entire design verification status within a dashboard
- Use batch mode and large-scale processing and visualization

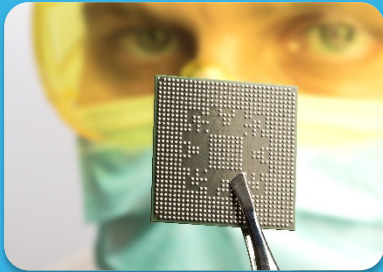


Removes the guesswork from analog electrical verification

But there are more engineers on the project

Two additional engineers could benefit from tools designed for specific tasks

Block Engineer/Chip Architect



- Should be able to use multiple testbenches to explore all circuit conditions and their impact on specifications
- Requires spec-driven, GUI-based, and scripting tools
- Needs more extensive variation-analysis tools

BUT...

- Re-use as much of the existing ADE XL code for stability and to reduce learning curves but make surgical changes to provide expanded usability

Circuit Engineer



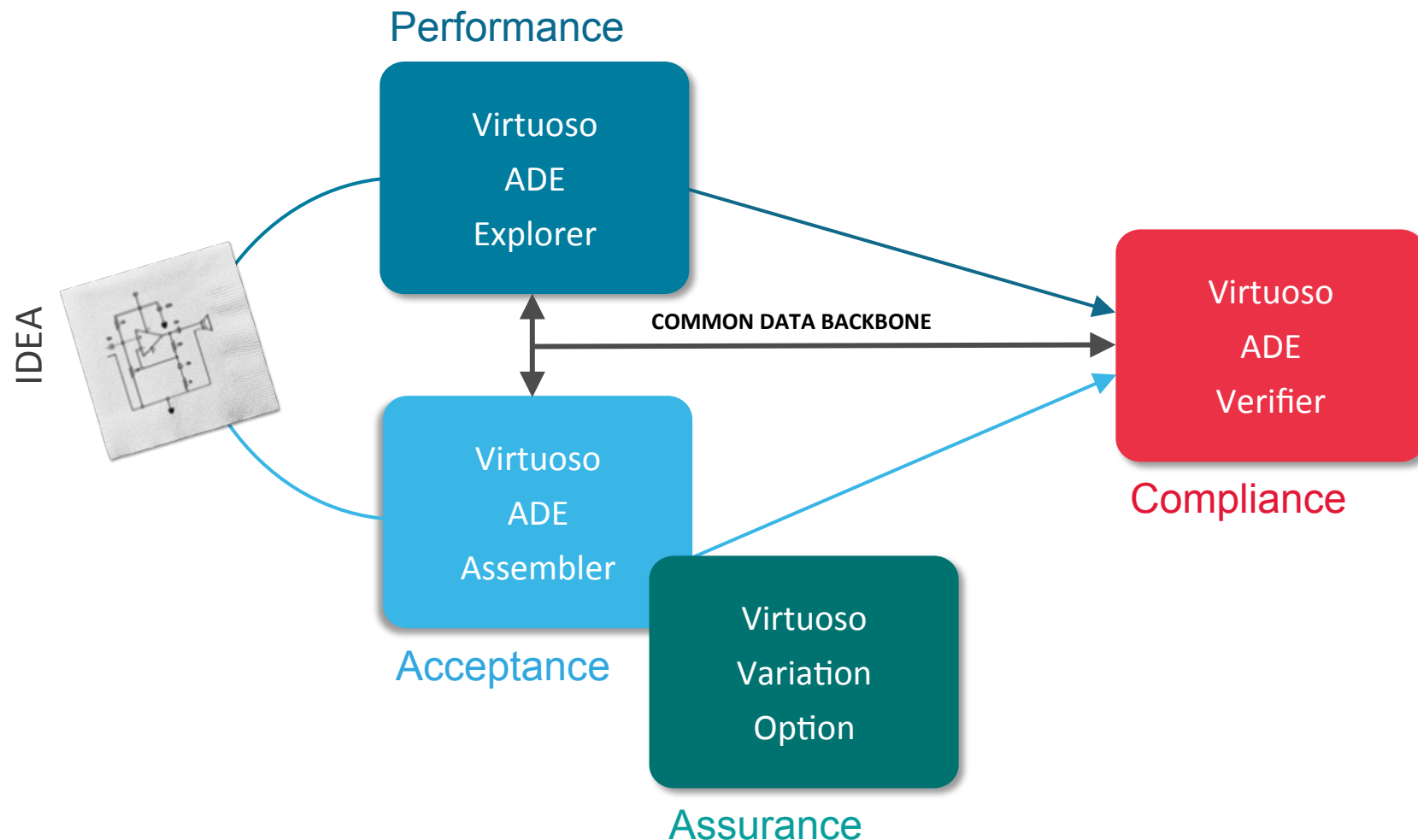
- Needs interactive, simple, fast tools that lend themselves to “self-learning”
- Ability to explore “what-if” conditions using design variables, usually one testbench with many measurements
- “Light” corner and statistical analysis at the engineers fingertips

BUT...

- Don't lose 25 years of ADE L “know-how” or performance improvements while creating a tool that takes analog design to the next level

Enhancing the Virtuoso ADE product suite

Reimagining analog design with emphasis on usability, performance, and innovation



Enhancing the Virtuoso ADE product suite

Virtuoso ADE Explorer

- At a glance:
 - Combined the simplicity of Virtuoso® ADE L with some of the most useful features from Virtuoso ADE XL into a highly interactive, single testbench analyzer that assists engineers at the earliest stages of circuit design to get the design right
- User benefits:
 - Monte Carlo and corners analysis included along with corner derivation from statistical sampling. No additional 3rd party tools are required at the base level. All the variation tools needed are integrated into a single cockpit.
 - Interactive device tuning mode using the Spectre® family of simulators returns answers in a flash
 - On-schematic use model employing pull-downs, waveform balloons and docked assistants to create a “one-window-only” high-performance visual environment
 - Spectre checks and asserts assistant detects static and dynamic electrical glitches that can cause failures during simulation, so users don’t have to wade through gigabytes of data

Virtuoso ADE Explorer

Expanded view to show corner results in a datasheet

The screenshot displays the Virtuoso ADE Explorer interface for a project named "Two_Stage_Opamp OpAmp_AC_top maestro". The interface includes a menu bar, a toolbar, and a left-hand pane with a tree view of analysis settings. The main area shows a "Results" tab with a table of corner analysis results.

Left Pane Tree View:

- AC
 - Simulator: spectre
 - Analyses
 - dc t
 - ac 1 10G Automatic Start-Stop
 - xf 1 1G 10 Logarithmic Points Per De.
 - Design Variables
 - M7_M6_fingers_ratio 12
 - M8_M6_fingers_ratio 9
 - M9_M10_fingers_ra... 1
 - cload 500f
 - rload 1000
 - vdd 1.4
 - Parameters
 - CornerRadius
 - Nominal
 - C0
 - Monte Carlo Sampling

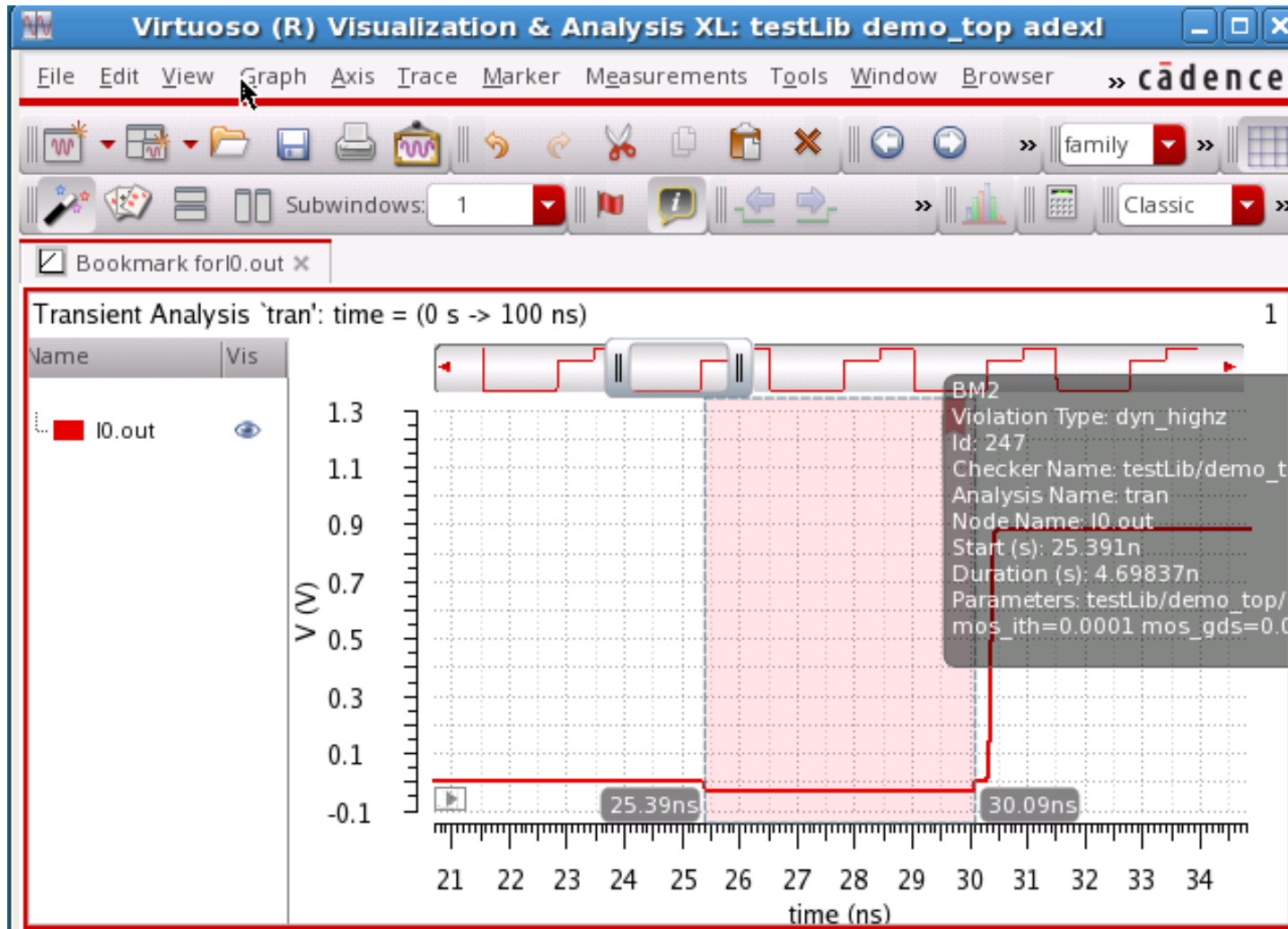
Results Table:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3	C0_4
AC	/V1/PLUS											
AC	/OUT											
AC	Op_Region	0				0	0	0	0	0	0	0
AC	Current	1.163m	< 1.2m		near	1.163m	1.262m	1.198m	1.189m	1.23m	1.219m	1.262m
AC	UGF	482.7M	> 450M		fail	401.2M	538.2M	509.7M	401.2M	524.5M	414.2M	538.2M
AC	Gain	47.4	> 48		near	46.13	49.12	48.14	46.13	48.65	46.64	49.12
AC	Voffset	1.783m	range 1m 5m		pass	1.546m	2.336m	1.662m	2.336m	1.601m	2.226m	1.546m
AC	GainCm	-1.636				-5.769	-555.5m	-3.058	-555.5m	-4.347	-1.787	-5.769
AC	CMRR	49.04	> 50		near	46.68	54.89	51.2	46.68	53	48.42	54.89
AC	GainVsupply1	-6.533				-10.72	-4.434	-8.046	-4.434	-9.314	-5.624	-10.72
AC	PSRR	53.94	> 50		pass	50.56	59.84	56.18	50.56	57.97	52.26	59.84

Status Bar: T=27 C | Simulator: spectre | State: active

Virtuoso Visualization and Analysis Window

Analyzing Spectre checks in the waveform



Enhancing the Virtuoso ADE product suite

Virtuoso ADE Assembler

- At a glance:
 - An interactive, multi-testbench environment that is designed to pull together all the parts of the design and their various specs to begin centering the design for manufacturing. Builds upon **Virtuoso® ADE Explorer**.
- User benefits:
 - Mini verification plans for creating conditional simulations with *drag-and-drop* simplicity opens up faster ways to do single-user regression testing
 - Improved regression scripting with simplified language for clarity
 - Both local and global optimization algorithms to aid design centering are included
 - Ability to develop worst-case corners from defined corner sets and to size (optimize) device parameters over those corners
 - Design migration for moving designs from one process to another enables reuse

Virtuoso ADE Assembler

Expanded to show run plans

The screenshot displays the Virtuoso ADE Assembler interface for editing a Two_Stage_Opamp OpAmp maestro. The interface includes a menu bar, a toolbar, and several panels. The 'Run Plan' panel on the right shows a hierarchical view of the simulation setup, including 'Single Run, Sweeps and Corners', 'Tests', 'Global Variables', 'Parameters', and 'Corners'. The 'Global Variables' section lists parameters like rload, vdd, macSw, and load with their respective values. The 'Parameters' section lists Run.0 and Run.1. The 'Corners' section lists Monte Carlo Sampling. The 'Tests' section lists Global Variables, Parameters, and Corners.

The 'Data View' panel on the left shows a tree structure of the design, including Tests, Global Variables, Parameters, Corners, Documents, Setup States, Reliability Analyses, and Checks/Asserts. The 'Run Summary' panel shows 2 Tests, 4 Point Sweeps, 2 Corners, and a Nominal Corner.

The 'Outputs Setup' panel shows a table of 15/36 rows with columns: Test, Name, Type, Details, EvalType, Plot, Save, and Spec. The table lists various simulation results, including signal levels, settling time, phase margin, and current levels.

Test	Name	Type	Details	EvalType	Plot	Save	Spec
TRAN	myOut	signal	/OUT	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
TRAN	Swing	expr	(value(VT("/OUT")) 2.5e-08) - ...	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	> 0.98
TRAN	RelativeSwingPercent	expr	((Swing / VAR("/vdd")) * 100)	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	> 75
TRAN	SettlingTime	expr	settlingTime(VT("/OUT")) 0 t 2...	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	< 10n
TRAN	PhaseMargin	expr	getData("/phaseMargin" ?res...	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	> 10
TRAN		signal	/IO/net6	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
TRAN		signal	/IO/net10	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
AC	Current	expr	abs(IDC("/V1/PLUS"))	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	< 1.5m
AC		signal	/V1/PLUS	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
AC		signal	/OUT	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
AC	UGF	expr	cross(dB20(mag(VF("/OUT")))...)	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	> 533M
AC	Gain	expr	value(dB20(mag(VF("/OUT")))...)	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	> 46
AC	Voffset	expr	(VDC("/inm") - VDC("/inp"))	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	range -10m 10m
AC		signal	/inm	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
AC		signal	/inp	point	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

The 'History' panel at the bottom shows a list of items with columns for 'History Item' and 'Status'. The first item is 'plot new graph subwindow'.

Enhancing the Virtuoso ADE product suite

Virtuoso Variation Option

- At a glance:
 - Advanced statistical analysis for deeper circuit exploration, particularly at advanced nodes
- User benefits:
 - Fast Monte Carlo yield verification with sample reordering for performance
 - Special foundry APIs available for 16nm and below
 - One-step creation of worst-case 3-sigma corners makes calculating them easy
 - High yield estimation algorithm (>3 -sigma) has the right mathematics for developing the estimates without 10s of thousands of simulation runs
 - Statistical sensitivity and mismatch analyses which can aid the designer to pinpoint the troublemaker devices in the design
 - One-button yield improvement feature combines sensitivity, optimization, and device resizing all into a single process

Enhancing the Virtuoso ADE product suite

Virtuoso ADE Verifier

- At a glance:
 - For the first time, Cadence offers a Virtuoso® platform-based circuit verification environment that provides the starting point to bring a formal method to design verification of analog circuits
- User benefits:
 - Offers a complete regression environment for pulling together the entire set of analog blocks from all the engineers to ensure that nothing got missed in their operation
 - Sits *above* all of the analog test benches and allows for unique sequencing that may be required during final verification or regression simulations. No more guessing about the status of the design.
 - Provides an easy-to-read dashboard of the current signoff status of the analog blocks, removing any guesswork
 - Eases learning curve via multi-language support
 - Provides the bridge between the analog world and the more extensive and well-defined metric-driven digital flows

Virtuoso ADE Verifier

Mapping between the plan and implementations

The screenshot displays the Virtuoso ADE Verifier interface for a project named 'amsPLL TOP_verification verification*'. The overall progress is 35%, with a green bar indicating progress and a red bar indicating remaining work. The interface is divided into two main panels: 'Verification Requirements (87% Mapped)' and 'Verification Implementations (34% Mapped) [Prefer Verifier Spec and Check]'.

Verification Requirements (87% Mapped)

ID	Title	Goal	Min	Max	Units	Description
ID1.2.3	Slew Rate	Spec Pass				Slew Rate
ID1.3	Functional tests	Ran OK				Make sure that the block is functional
ID1.4	Power up behavior	Spec Pass				Do a proper power up sim on full tra
ID1.5	Ensure Yield	Note				
ID1.5.2	Overall Yield	Spec Pass	75			The overall yield for this circuit shou
AS1	No Assertion Failure	Spec Pass		1		
ID2	Filter	Note				The filter is a digital filter implementa
ID3	Power Amp	Note				Power amp for the output
ID4	VCO	Note				VCO for the PLL of the SAD project w
ID4.1	vcontrol/freqout beh	Spec Pass	0	1.5e8		The output frequency of the VCO shou
ID4.2	max_current	Spec Pass		70m	A	The peak current limit is at 8m A
ID4.3	Power consumption	Spec Pass		0.008		The power consumption of this block
ID4.6	PD power consumption	Spec Pass		800u		Imported requirement from:
ID4.4	PD behavior	Spec Pass	1.8	2.1		The PD pin is active high.
ID4.5	Startup	Manual				The startup must happen after the fi
AS2	no circuit check / assertion failing	Spec Pass		1		

Verification Implementations (34% Mapped) [Prefer Verifier Spec and Check]

Hier	Run	Output	Specification	Units	Mapped
		DCGain	>25		ID1.1.2
		MAC_DCGain	>20		ID1.1.1
Test:		opamp090:full_diff_opamp_TRAN:1			100%
		SettlingTime	None		ID1.2.2
		SlewRate	>125M		ID1.2.3
		Count 'All Checks/Asserts'	<1		AS1
Cellview:		opamp090/full_diff_opamp_AC/maestro_MC/Active			5%
Test:		opamp090:full_diff_opamp_AC:1			5%
		opamp090:full_diff_opamp_AC:1:Overall_Yield	None		ID1.5.2
		DCGain::Yield	None		No
		DCGain::Mean	None		No
		DCGain::StandardDeviation	None		No
		DCGain::Cpk	None		No
Cellview:		amsPLL/PLL_VCO_320MHZ_tb/maestro/Active			75%
Test:		amsPLL:PLL_VCO_320MHZ_tb:1			75%
		avg_current	<8m		ID4.3
		max_current	<70m	A	ID4.2
		freq_check	Spec Chec...	Hz	ID4.1
Cellview:		amsPLL/PLL_VCO_320MHZ_PD_tb/maestro/Active			100%
Test:		amsPLL:PLL_VCO_320MHZ_tb:1			100%
		avg_current	<800u		ID4.6
		output_low	1.8 to 2.1		ID4.4
		assertions	<1		AS2

The interface includes a 'Show Cross Mapping at Cursor' checkbox and a 'Map' button. The bottom status bar shows the Cadence logo.



Virtuoso Layout Suite enhancements

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What are we announcing?

Cadence® Virtuoso® Layout Suite

- Virtuoso Layout Suite L/XL
 - New patented graphics rendering provides 10X-100X accelerated performance while zooming, panning, dragging, and drawing large layouts
 - New dynamic measurement, dynamic net labeling, and smart auto via provide 10X accelerated productivity
 - New transparent hierarchy provides more flexible schematic-driven layout creation and manipulation, bringing connectivity-driven layout productivity to more custom layout design styles
- Virtuoso Layout Suite GXL
 - New ModGen interactive pattern manipulation flow makes real-time customization of ModGens very visual and simple
 - New structured device-level routing (pin-to-trunk) space-based router algorithms increase productivity by as much as 50 percent

*These tools are seamlessly integrated with our
Virtuoso Schematic Editor and Virtuoso Analog Design Environment
suite of tools*

Summary

The new next-generation Virtuoso platform technologies provide the next logical evolution in analog design

- **Usability**

- Features logically designed to be at the engineer's fingertips without being intrusive at each step of the design cycle
- Easy to set up and automate multiple testbenches and regressions

- **Performance**

- Using the power of the Spectre® simulator's deep integration within the environment, interactive tuning and in-simulator device checks find the errors fast, reducing debug time by 50% for these problems; no more hunt and peck and hope
- The new graphics rendering engines in Virtuoso® Layout Suite are improved by 10X-100X, making it easy to navigate the densest layouts
- Enhanced structured, device-level routing algorithms improve productivity by as much as 50%

- **Innovation**

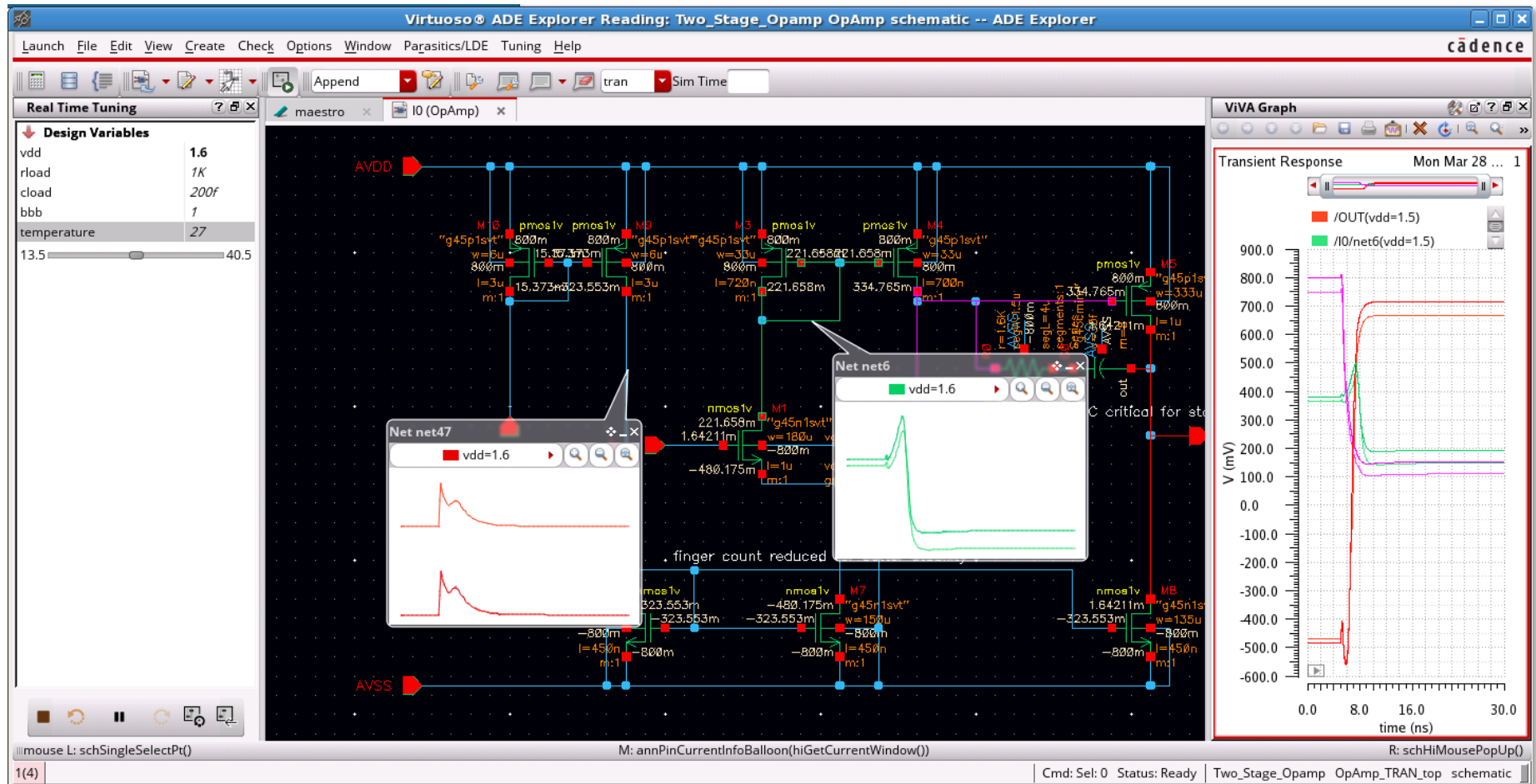
- Analog electrical design verification has now become an industry reality; goodbye to the *"Why didn't you tell me you changed that?"* conversations
- Reduce/eliminate over-margining by addressing design and process variation



Additional Screenshots

Virtuoso ADE Explorer interactive tuning mode

Provides the fastest performance using Cadence Spectre family of simulators



Virtuoso ADE Verifier

Mapping between the plan and implementations

The screenshot displays the Virtuoso ADE Verifier interface for a project named "amsPLL TOP_verification verification*". The interface is divided into two main panels: "Requirements (83% Mapped)" on the left and "Implementations (24% Mapped)" on the right. The top status bar shows an "Overall Progress" of 42%.

Requirements (83% Mapped)

Hier	Title	Type	MinSpec	MaxSpec	Unit	Description
1	Analog V...	Note				This is the new project "Analog Verification Project" for customer XYZ...
1.1	OpAmp	Note				This is a classical OpAmp design coming from our team in Japan (汎用...
1.1.1	Analog Pa...	Note				Ensure the AC behavior
1.1.1.1	Voffset	Spec Pass	-10m	10m	V	Input voltage offset
1.1.1.2	Gain	Spec Pass	47		dB	Nominal open loop gain value
1.1.1.3	UGF	Spec Pass	533M		Hz	unity gain frequency. This should be measured by ...
1.1.1.4	Current	Spec Pass		1.5m	A	Maximum current consumption
1.1.2	Analog Pa...	Note				Ensure correct tran beh.
1.1.2.1	PhaseMa...	Spec Pass	20		d...	Title: PhaseMargin
1.1.2.2	RelativeS...	Spec Pass	75		%	Title: RelativeSwingPercent
1.1.2.3	SettlingTi...	Spec Pass		8n	s	Settling time is less important in this case because ...
1.1.2.4	Swing	Spec Pass		980m		The swing is critical for this project. It should be verified in detail ove...
1.1.3	Function...	Ran OK				Make sure that the block is functionally correct.
1.1.4	Power up...	Ran OK				Do a proper power up sim on full transistor level. The results should b...
1.1.5	Ensure Yl...	Note				
1.1.5.1	Overall A...	Spec Pass	95			The overall yield for this circuit should be above 95%.
1.1.5.2	Overall T...	Spec Pass	95			The overall yield for this circuit should be above 95%.
1.2	Filter	Note				The filter is a digital filter implementation using ...
1.3	Power A...	Note				Power amp for the output
1.4	VCO	Note				VCO for the PLL of the SAD project which will be added later.
1.4.1	vcontrol/...	Spec Pass	0	150M	Hz	The output frequency of the VCO should be above the following limit:
1.4.2	max_curr...	Spec Pass		70m	A	The peak current limit is at 8m A

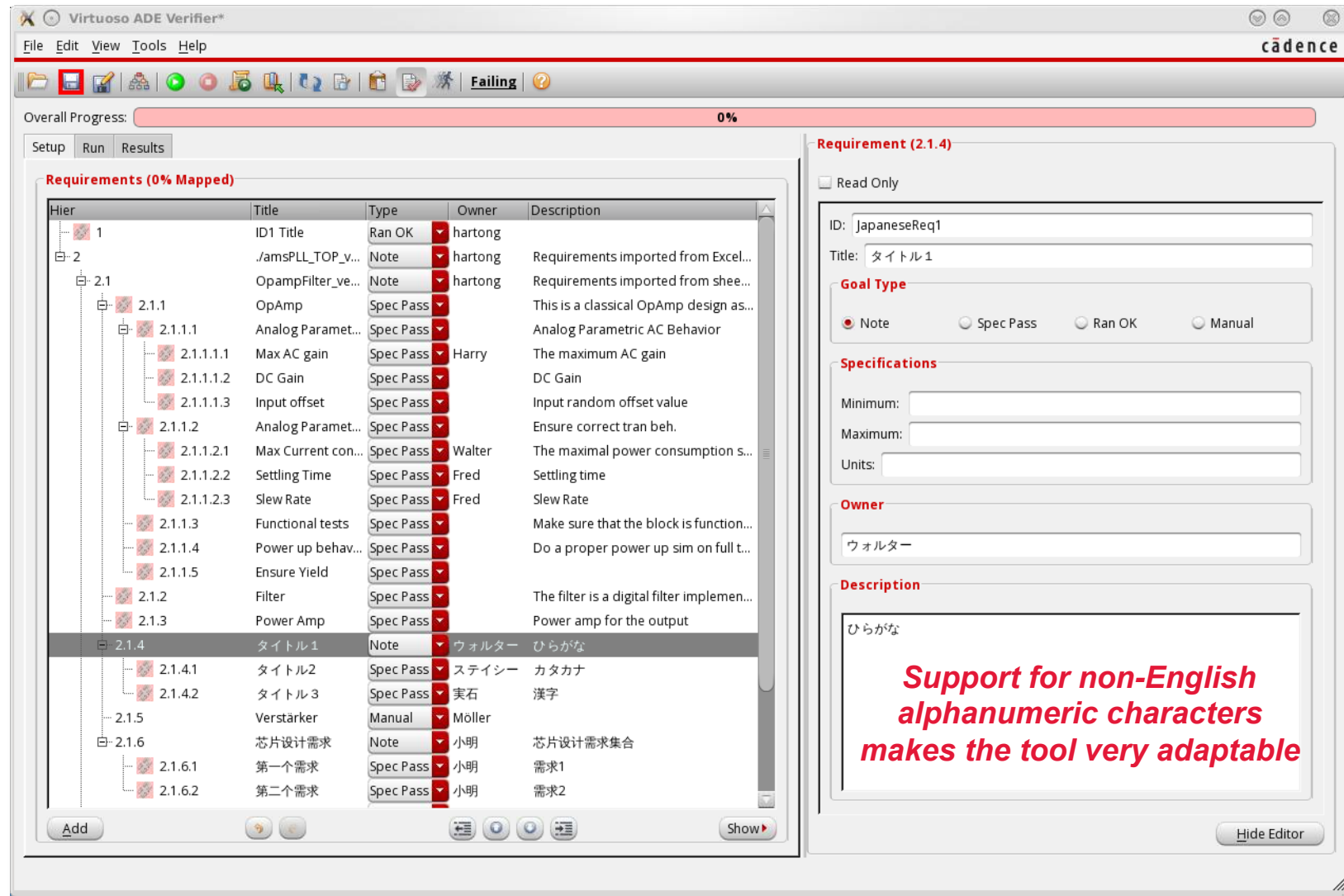
Implementations (24% Mapped)

Hier	History	Run	Output	Specification	Units	Mapped
Cellview:	Active	✓	Two_Stage_Opamp/OpAmp/maestro_nominal/Active			80%
Test:			AC			100%
Test:			TRAN			67%
Swing				>0.98		1.1.2.4
SettlingTime				<8n	s	1.1.2.3
RelativeSwingPercent				>75	%	1.1.2.2
PhaseMargin				>20	degree	1.1.2.1
phase(VF("OUT"))				None		No
mag(VF("OUT"))				None		No
Cellview:	Active	✓	Two_Stage_Opamp/OpAmp/maestro_MC/Active			5%
Test:			AC			5%
Output Values						
UGF				>533M	Hz	No
Statistical Values						
AC::Overall_Yield				None		1.1.5.1
UGF::StandardDeviation				None		No
UGF::Yield				None		No
Test:			TRAN			5%
Output Values						
Statistical Values						
TRAN::Overall_Yield				None		1.1.5.2
PhaseMargin::Yield				None		No

The interface includes a "Show Cross Mapping at Cursor" checkbox and a "Map" button at the bottom.

Virtuoso ADE Verifier

Support for non-English characters eases adoption of the tool



cā dence[®]