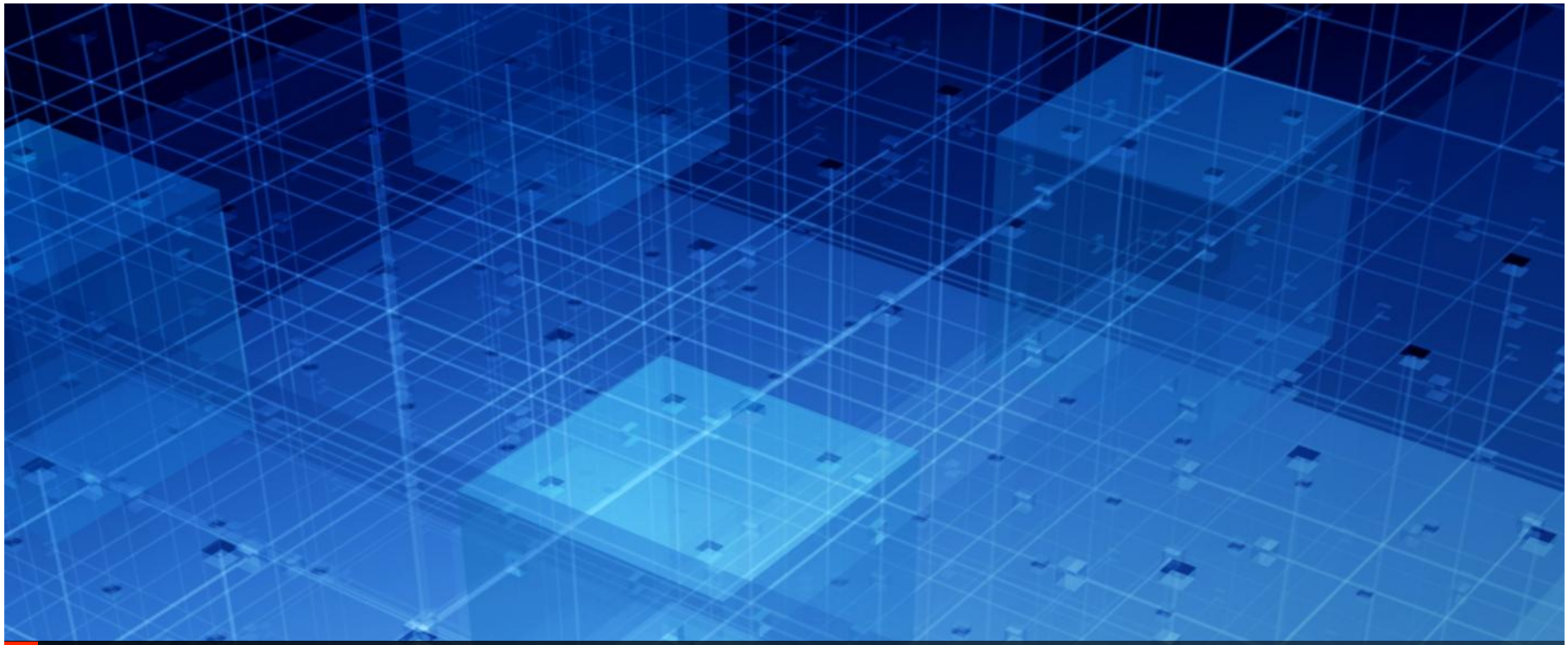

Next-Generation Virtuoso Platform: Welcome to the New Sound of Analog Design

EMBARGOED UNTIL APRIL 5th (7:45 AM PST)

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What are we announcing?

Cadence® Virtuoso® ADE Product Suite

- Virtuoso ADE Explorer
  - Built for performance to get the analog circuit up and running in the initial stages of the design cycle
- Virtuoso ADE Assembler
  - Built for handling numerous acceptance tests for the design under various environmental conditions
- Virtuoso Variation Option
  - Built to assure accurate variation analysis is done for advanced nodes and high-yield products
- Virtuoso ADE Verifier
  - Built to provide electrical verification compliance status for all of the analog blocks being designed and coalesced into a single design

These tools work in parallel with our existing Virtuoso Analog Design Environment L, XL, and GXL suite of tools

The Analog Verification Problem: What's Needed Across Different Industries?

Let’s look at verification for functional safety
Automotive

- Traceability
- Specification linkage
- Change management
- Reproducible results

Requirement-driven SoC verification

- Fault injection
- Fault simulation
- Multiple abstractions
- Safety reports

Verification for functional safety (ASIL)

ISO 26262

Medical devices are highly regulated

A failure here could mean life or death

- 1 general standard
- 10 collateral standards
- 60 particular standards
- Traceability is key to each

Set of applicable standards

- Package integrity tests
- Failure modes and effects analysis
- Thermal analysis
- Worst-case analysis

Examples of FDA demanded verification methods*

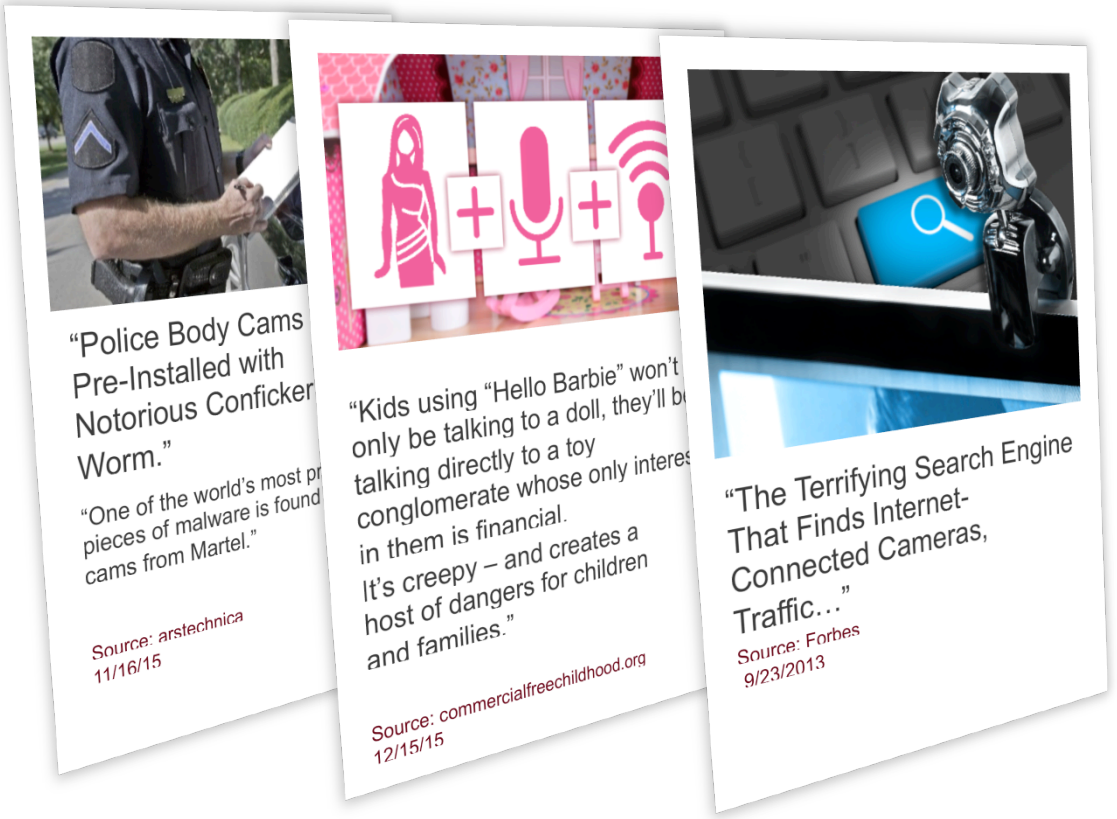
IEC 60601**
IEC 62304**

Government Regulatory Agencies

FDA:	United States
EMA:	Europe
PMDA:	Japan
CFDA:	China
CDSCO:	India

*FDA: ***Design Control Guidance For Medical Device Manufacturers***
** 60601 Medical Electronics and 62304 Software contained within

IoT
Security verification is unfolding



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Customers need to make analog/mixed-signal verification *traceable*

Medical
IEC 62304
2006

Aviation
DO-254
2006

Automotive
ISO 26262
2012

Industrial
IEC 61508
1998

FDA: ***Design Control Guidance For Medical Device Manufacturers***

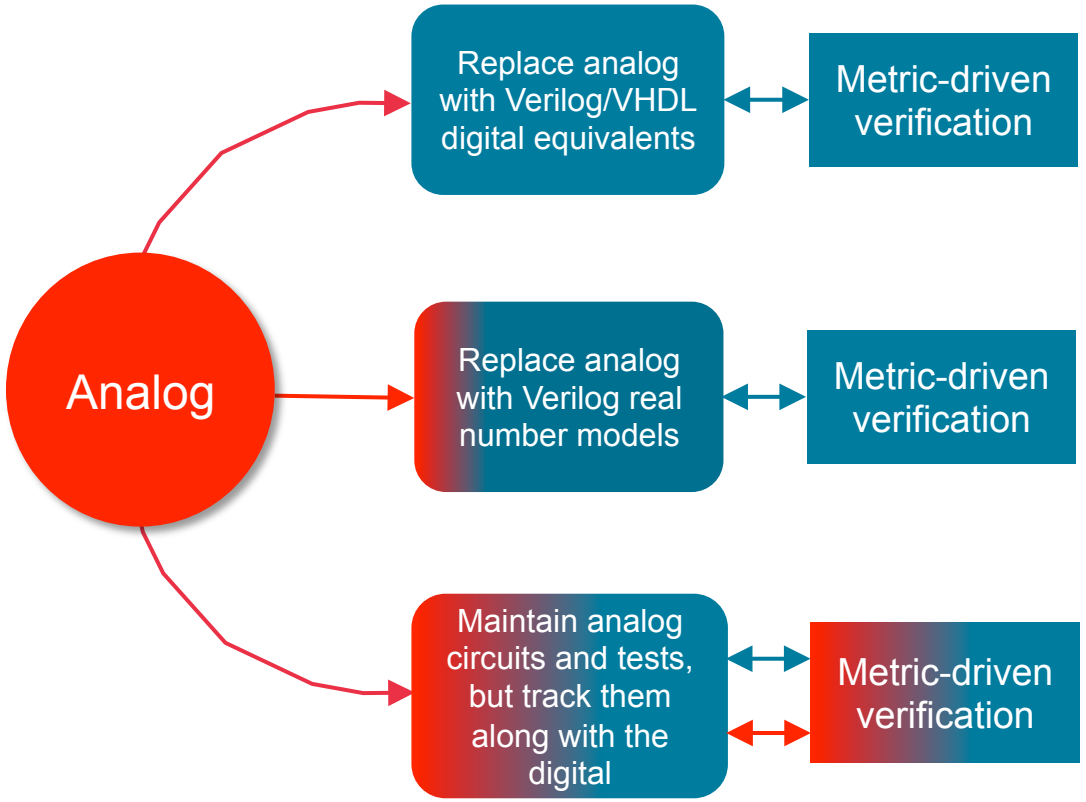
The results of the design verification, including identification of the design, method(s), the date, and the individual(s) performing the verification, shall be ***documented in the Design History File****.*

In the consumer industry, “first-time right” is key and failures of a large mixed-signal chip due to analog problems are no longer acceptable.

The challenge is, how do you make the analog design traceable?

Crossing the verification chasm

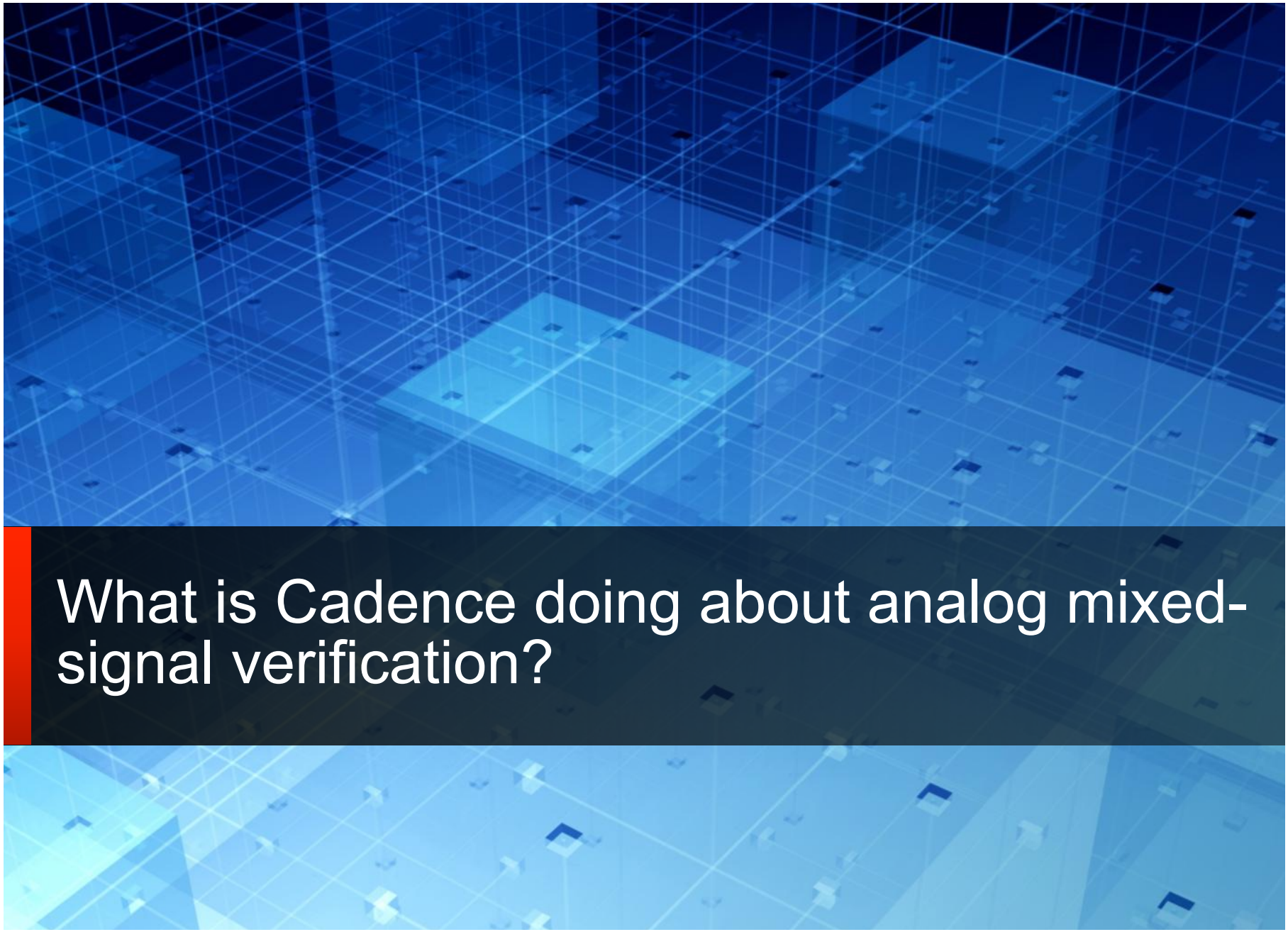
When it comes to mixed-signal, it is all about choices



This method keeps everything on a well-understood digital methodology, but the drawback is that all of the analog nature of the block is wiped out.

This method characterizes the analog behavior better and can provide simulation speed-up, but all of the physical effects impacts are lost.

*The **new** Virtuoso® ADE Verifier will give you analog details, but allow you to share the data more easily with the digital domain.*



What is Cadence doing about analog mixed-signal verification?

Analog design traceability
How is it done today?

- Lots of manual intervention to determine the state of “verification” for each block
  - Use of spreadsheets is prevalent, but they are disconnected from the software and, therefore, updates are easily missed

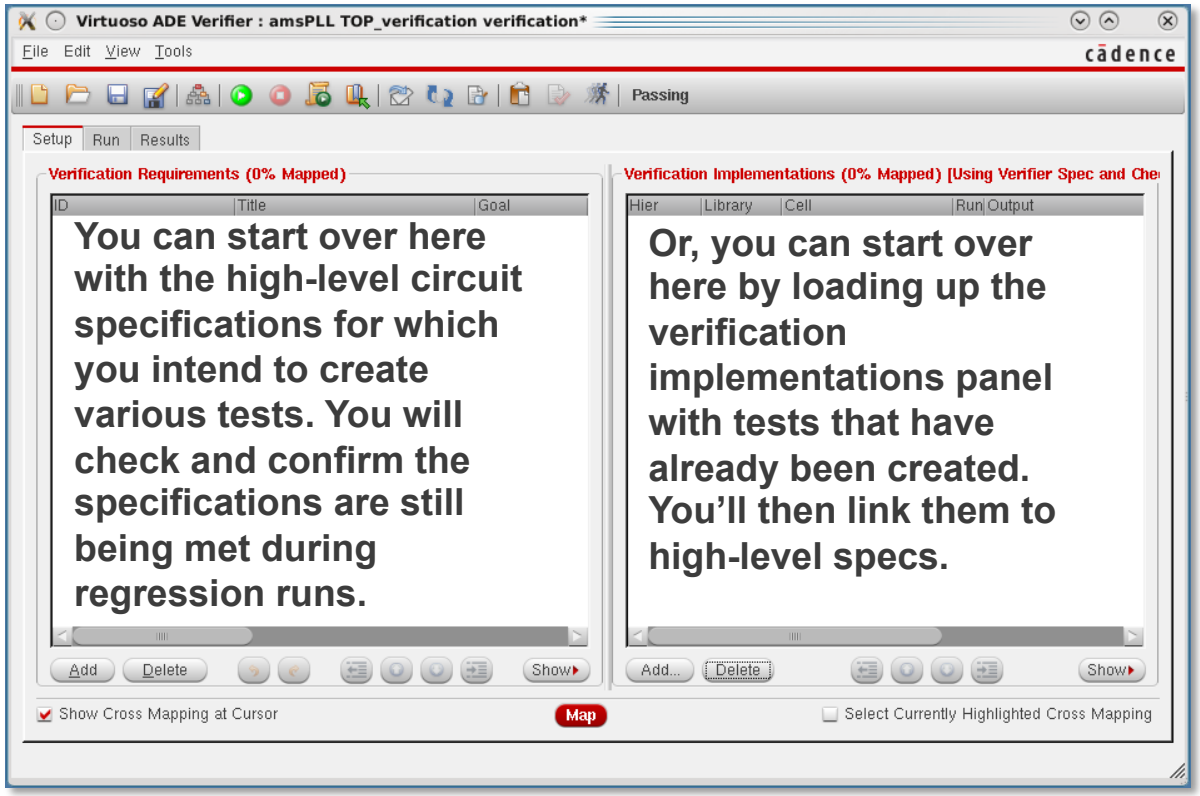
- Convert the analog to digital and use the standardized digital, metric-driven flows, hoping that the physical implementations don’t disrupt signal quality too much

- Sometimes homegrown solutions are built by CAD teams since EDA vendors hadn’t provided this capability to the analog world before

What Cadence provides in the next-gen Virtuoso platform

Verification Engineer/Project Lead

- Able to run 100s of complex, interdependent simulations
- Monitor job status with complete control over simulator queuing
- Get a quick overview of the entire design verification status within a dashboard
- Use batch mode and large-scale processing and visualization



Removes the guesswork from analog electrical verification

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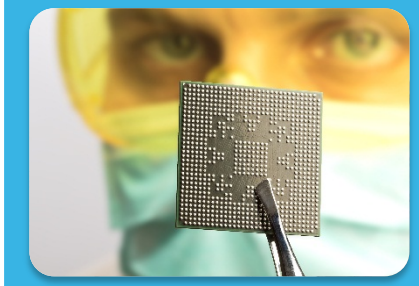
But there are more engineers on the project

Two additional engineers could benefit from tools designed for specific tasks

Block Engineer/Chip Architect

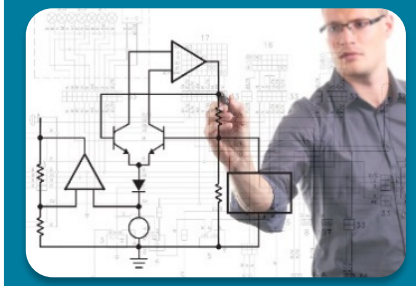


- Should be able to use multiple testbenches to explore all circuit conditions and their impact on specifications
- Requires spec-driven, GUI-based, and scripting tools
- Needs more extensive variation-analysis tools

BUT…

- Re-use as much of the existing ADE XL code for stability and to reduce learning curves but make surgical changes to provide expanded usability

Circuit Engineer



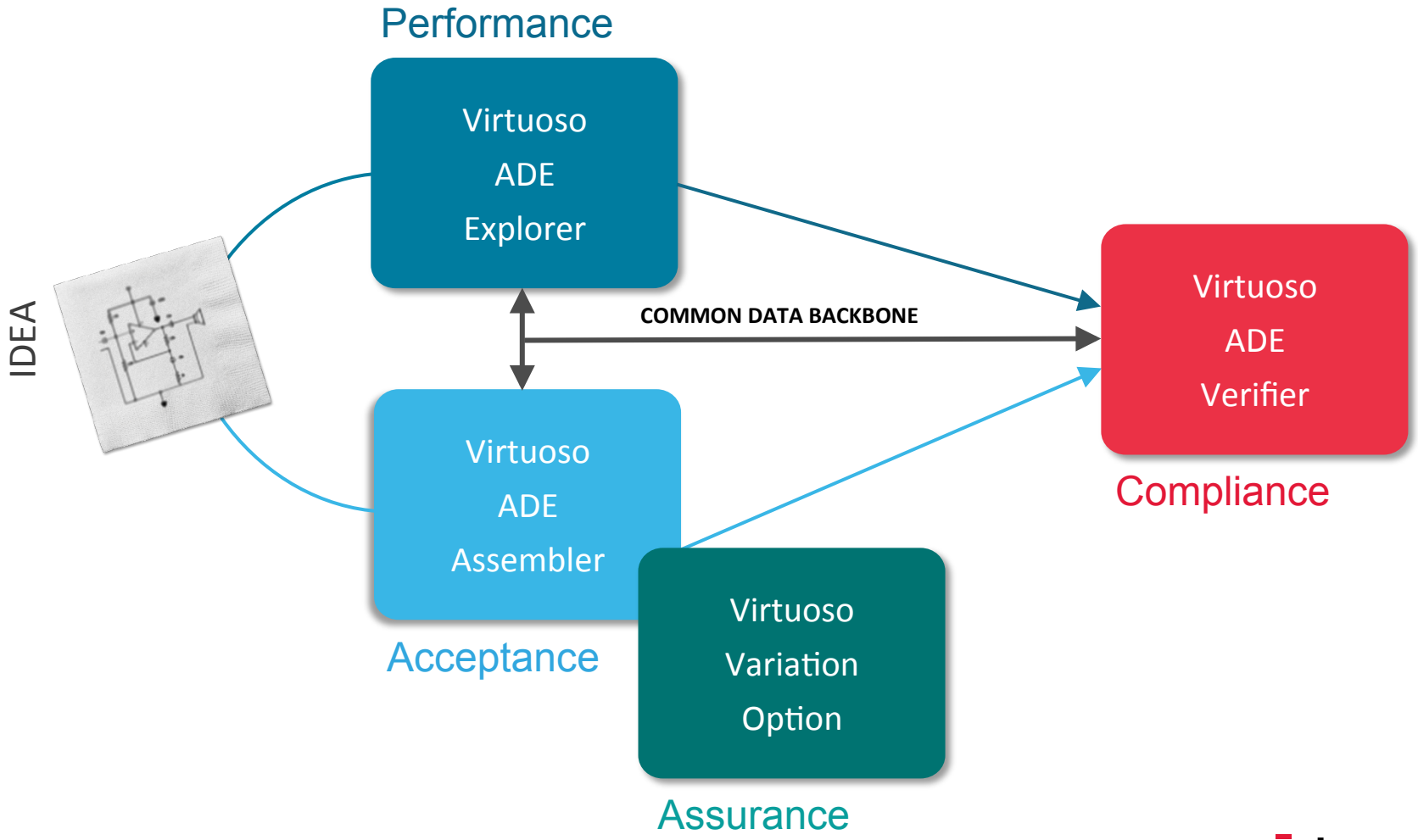
- Needs interactive, simple, fast tools that lend themselves to “self-learning”
- Ability to explore “what-if” conditions using design variables, usually one testbench with many measurements
- “Light” corner and statistical analysis at the engineers fingertips

BUT…

- Don’t lose 25 years of ADE L “know-how” or performance improvements while creating a tool that takes analog design to the next level

Enhancing the Virtuoso ADE product suite

Reimagining analog design with emphasis on usability, performance, and innovation



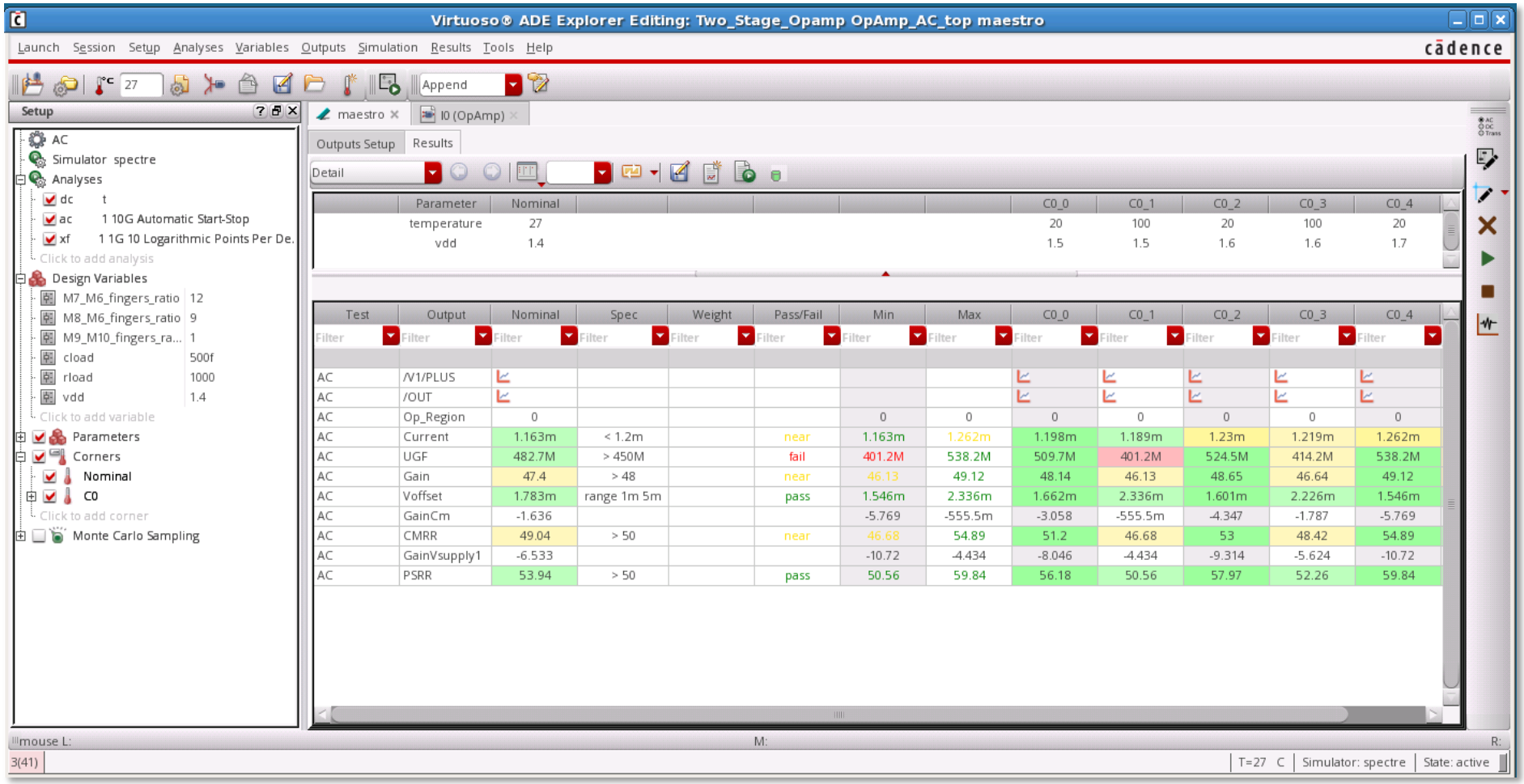
Enhancing the Virtuoso ADE product suite
Virtuoso ADE Explorer

- At a glance:
  - Combined the simplicity of Virtuoso® ADE L with some of the most useful features from Virtuoso ADE XL into a highly interactive, single testbench analyzer that assists engineers at the earliest stages of circuit design to get the design right

- User benefits:
  - Monte Carlo and corners analysis included along with corner derivation from statistical sampling. No additional 3rd party tools are required at the base level. All the variation tools needed are integrated into a single cockpit.
  - Interactive device tuning mode using the Spectre® family of simulators returns answers in a flash
  - On-schematic use model employing pull-downs, waveform balloons and docked assistants to create a “one-window-only” high-performance visual environment
  - Spectre checks and asserts assistant detects static and dynamic electrical glitches that can cause failures during simulation, so users don’t have to wade through gigabytes of data

Virtuoso ADE Explorer

Expanded view to show corner results in a datasheet



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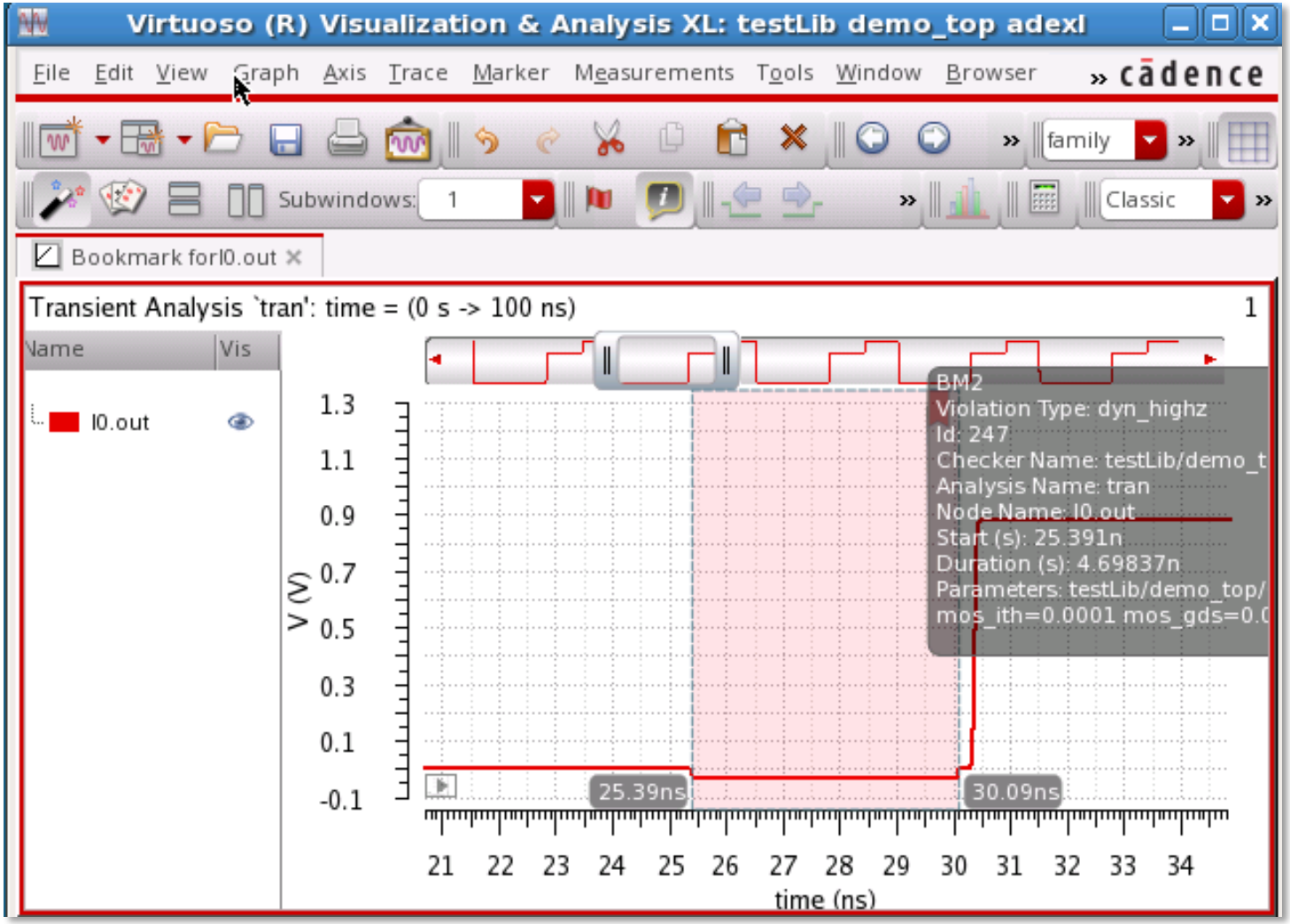
Virtuoso Visualization and Analysis Window

Analyzing Spectre checks in the waveform



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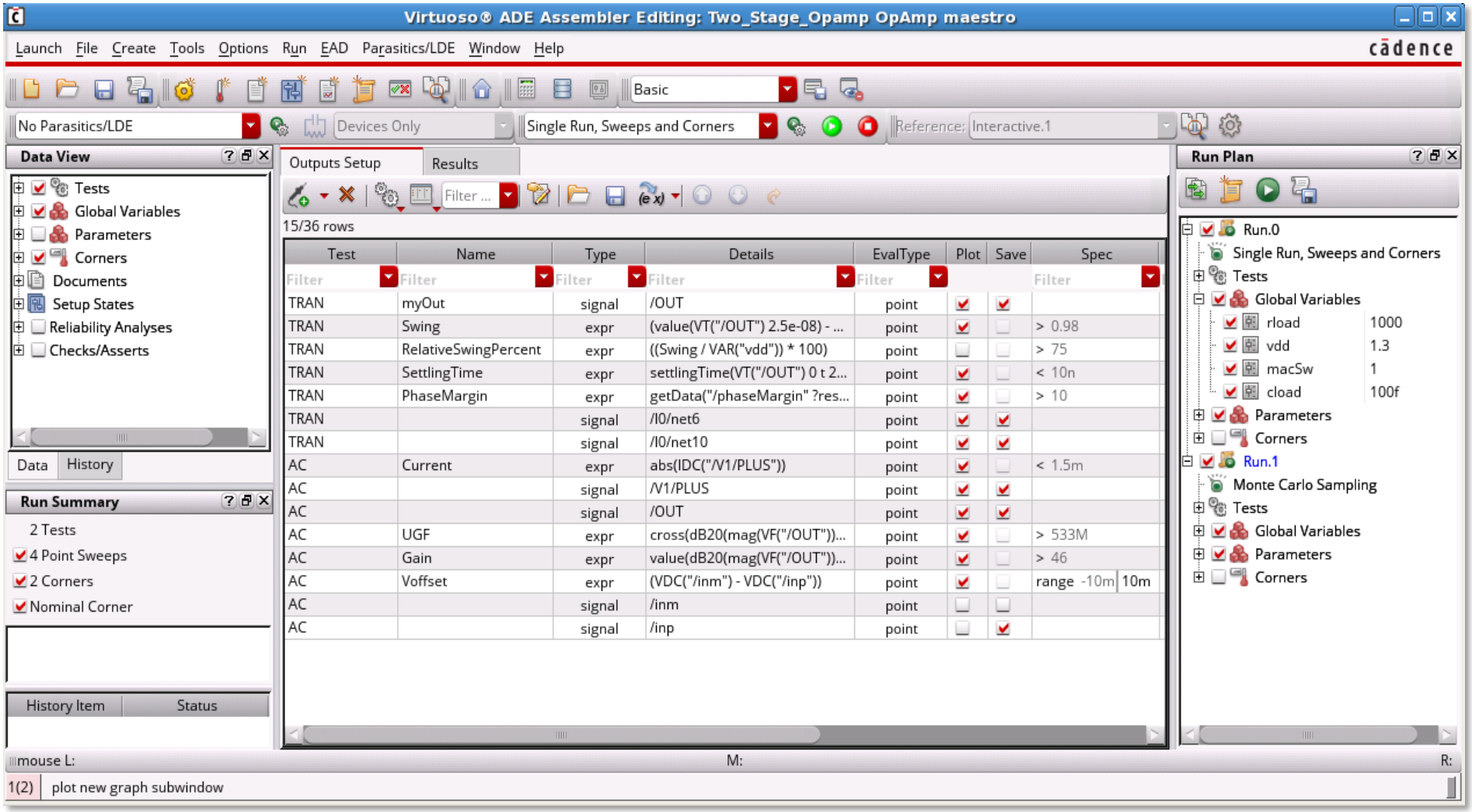
Enhancing the Virtuoso ADE product suite
Virtuoso ADE Assembler

- At a glance:
  - An interactive, multi-testbench environment that is designed to pull together all the parts of the design and their various specs to begin centering the design for manufacturing. Builds upon **Virtuoso® ADE Explorer**.

- User benefits:
  - Mini verification plans for creating conditional simulations with *drag-and-drop* simplicity opens up faster ways to do single-user regression testing
  - Improved regression scripting with simplified language for clarity
  - Both local and global optimization algorithms to aid design centering are included
  - Ability to develop worst-case corners from defined corner sets and to size (optimize) device parameters over those corners
  - Design migration for moving designs from one process to another enables reuse

Virtuoso ADE Assembler
Expanded to show run plans



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Enhancing the Virtuoso ADE product suite
Virtuoso Variation Option

- At a glance:
  - Advanced statistical analysis for deeper circuit exploration, particularly at advanced nodes

- User benefits:
  - Fast Monte Carlo yield verification with sample reordering for performance
    - Special foundry APIs available for 16nm and below
  - One-step creation of worst-case 3-sigma corners makes calculating them easy
  - High yield estimation algorithm (>3-sigma) has the right mathematics for developing the estimates without 10s of thousands of simulation runs
  - Statistical sensitivity and mismatch analyses which can aid the designer to pinpoint the troublemaker devices in the design
  - One-button yield improvement feature combines sensitivity, optimization, and device resizing all into a single process

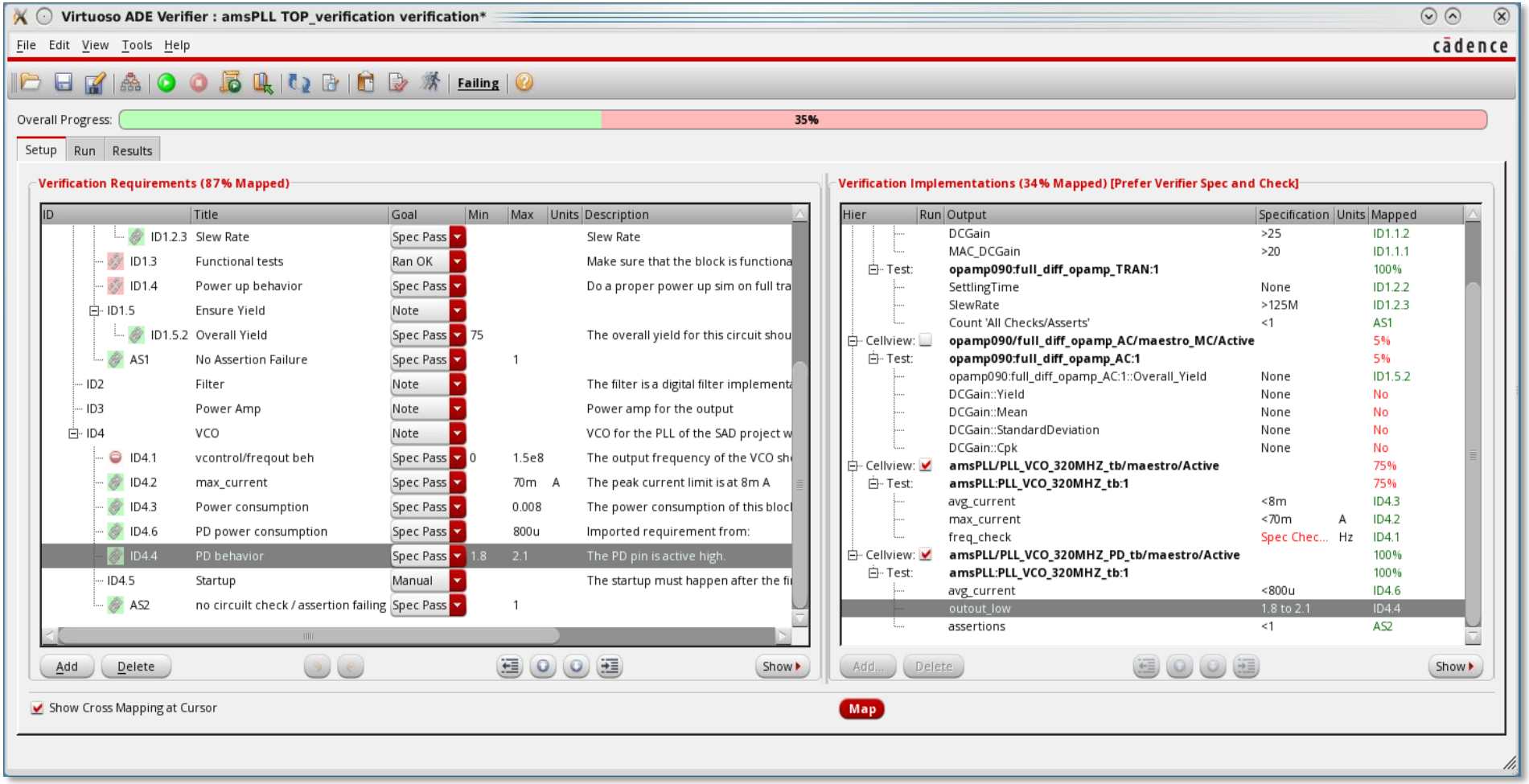
Enhancing the Virtuoso ADE product suite
Virtuoso ADE Verifier

- At a glance:
  - For the first time, Cadence offers a Virtuoso® platform-based circuit verification environment that provides the starting point to bring a formal method to design verification of analog circuits

- User benefits:
  - Offers a complete regression environment for pulling together the entire set of analog blocks from all the engineers to ensure that nothing got missed in their operation
  - Sits *above* all of the analog test benches and allows for unique sequencing that may be required during final verification or regression simulations. No more guessing about the status of the design.
  - Provides an easy-to-read dashboard of the current signoff status of the analog blocks, removing any guesswork
  - Eases learning curve via multi-language support
  - Provides the bridge between the analog world and the more extensive and well-defined metric-driven digital flows

Virtuoso ADE Verifier

Mapping between the plan and implementations



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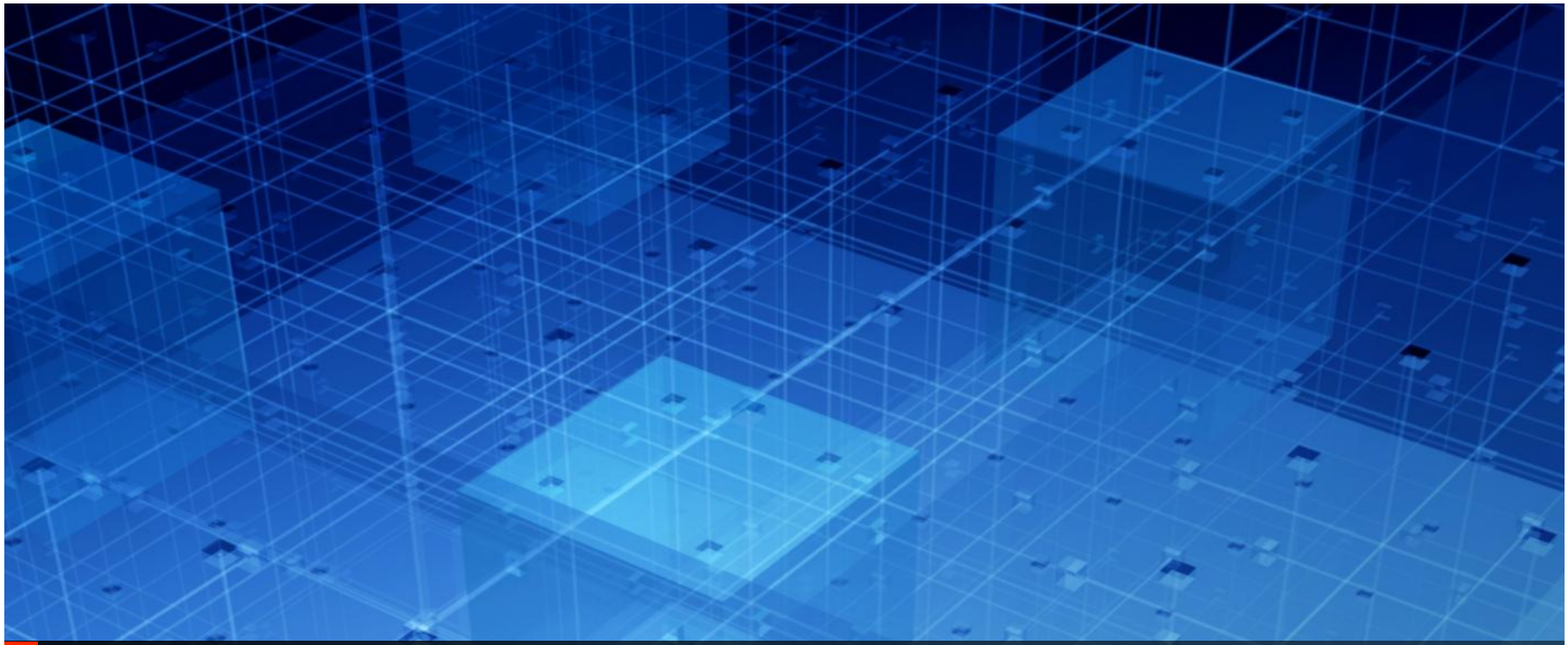

Virtuoso Layout Suite enhancements

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What are we announcing?

Cadence® Virtuoso® Layout Suite

- Virtuoso Layout Suite L/XL
  - New patented graphics rendering provides 10X-100X accelerated performance while zooming, panning, dragging, and drawing large layouts
  - New dynamic measurement, dynamic net labeling, and smart auto via provide 10X accelerated productivity
  - New transparent hierarchy provides more flexible schematic-driven layout creation and manipulation, bringing connectivity-driven layout productivity to more custom layout design styles
- Virtuoso Layout Suite GXL
  - New ModGen interactive pattern manipulation flow makes real-time customization of ModGens very visual and simple
  - New structured device-level routing (pin-to-trunk) space-based router algorithms increase productivity by as much as 50 percent

These tools are seamlessly integrated with our Virtuoso Schematic Editor and Virtuoso Analog Design Environment suite of tools

Summary

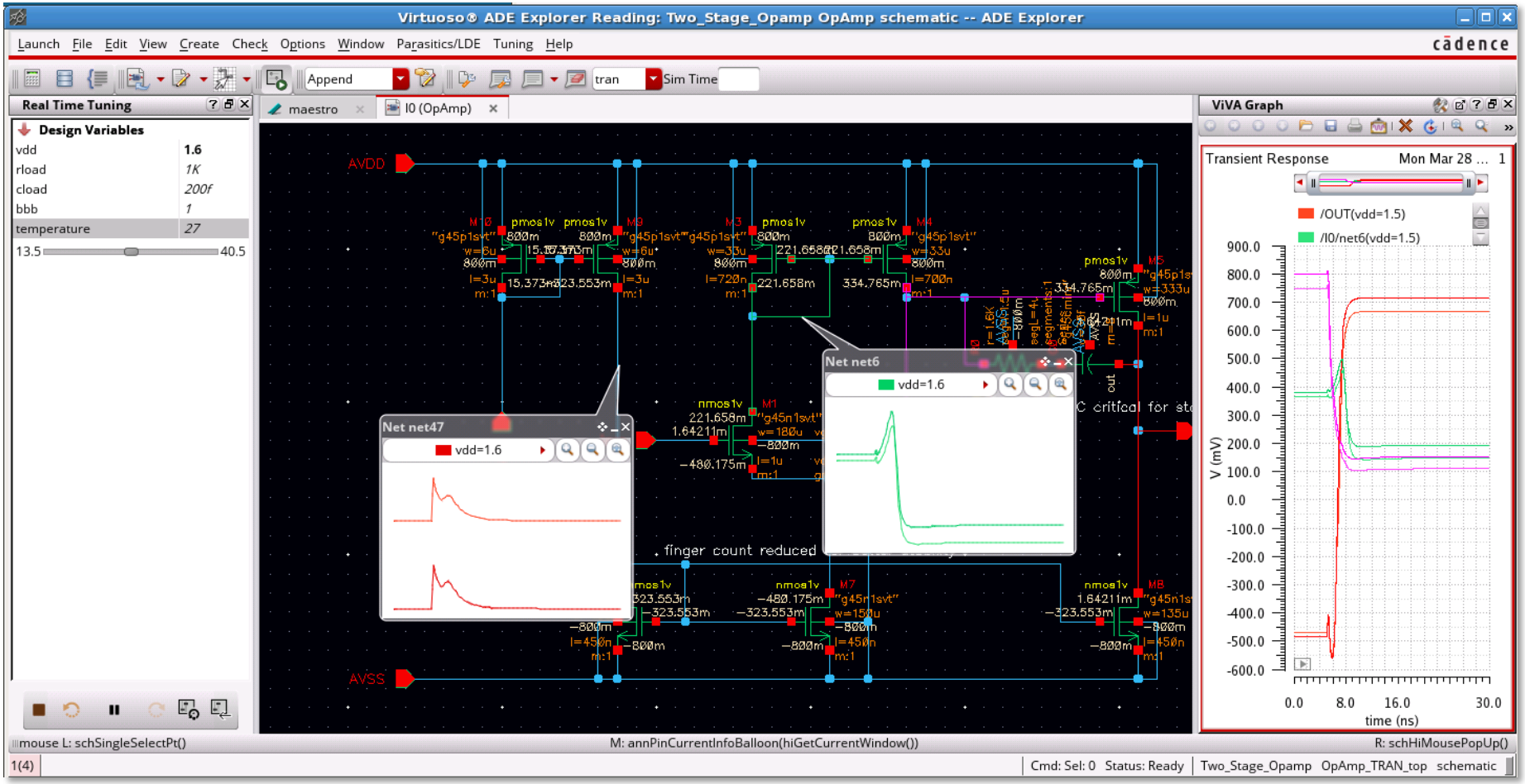
The new next-generation Virtuoso platform technologies provide the next logical evolution in analog design

- **Usability**
  - Features logically designed to be at the engineer's fingertips without being intrusive at each step of the design cycle
  - Easy to set up and automate multiple testbenches and regressions
- **Performance**
  - Using the power of the Spectre® simulator's deep integration within the environment, interactive tuning and in-simulator device checks find the errors fast, reducing debug time by 50% for these problems; no more hunt and peck and hope
  - The new graphics rendering engines in Virtuoso® Layout Suite are improved by 10X-100X, making it easy to navigate the densest layouts
  - Enhanced structured, device-level routing algorithms improve productivity by as much as 50%
- **Innovation**
  - Analog electrical design verification has now become an industry reality; goodbye to the *"Why didn't you tell me you changed that?"* conversations
  - Reduce/eliminate over-margining by addressing design and process variation

Additional Screenshots

Virtuoso ADE Explorer interactive tuning mode

Provides the fastest performance using Cadence Spectre family of simulators



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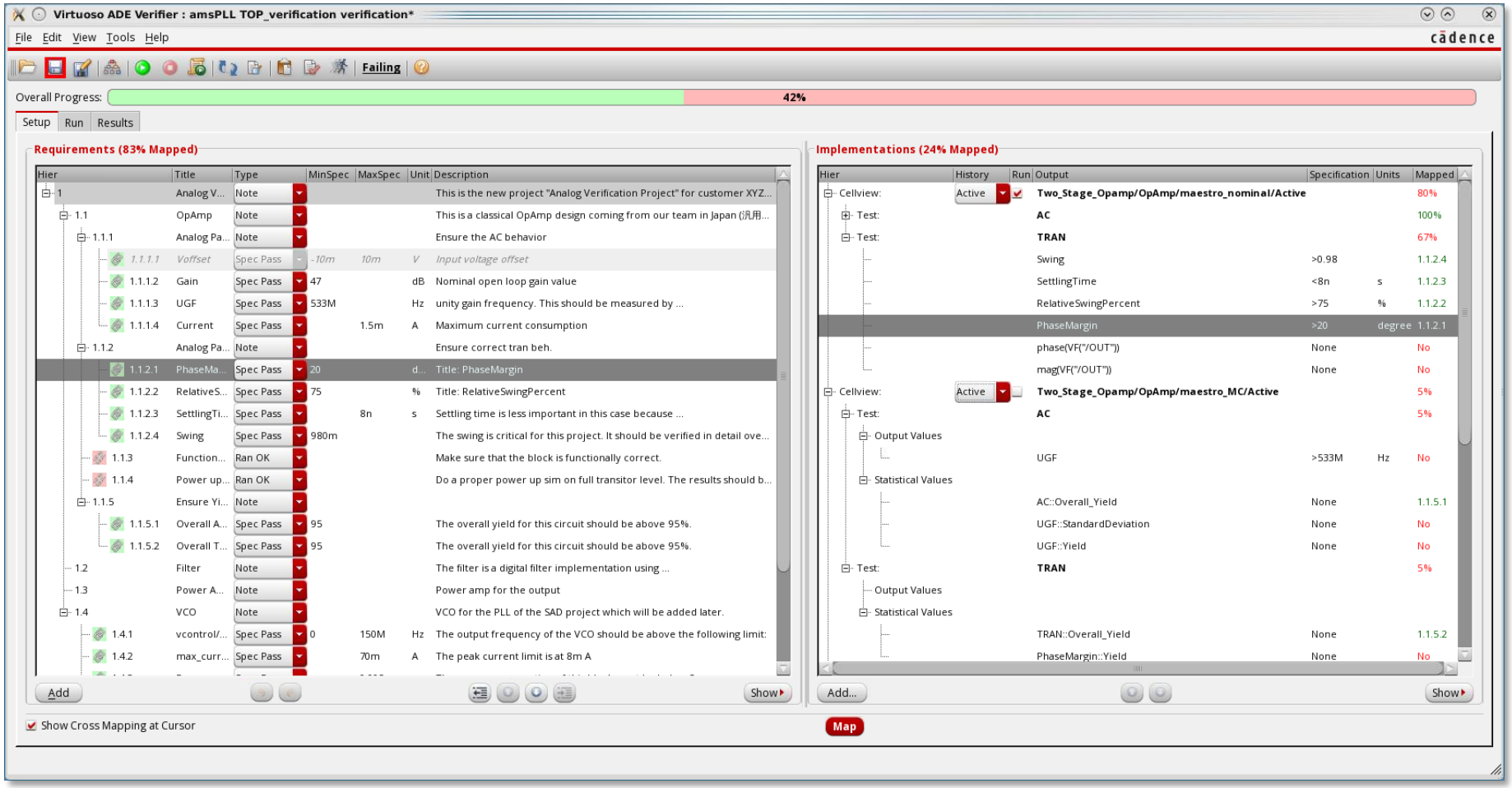
Virtuoso ADE Verifier

Mapping between the plan and implementations



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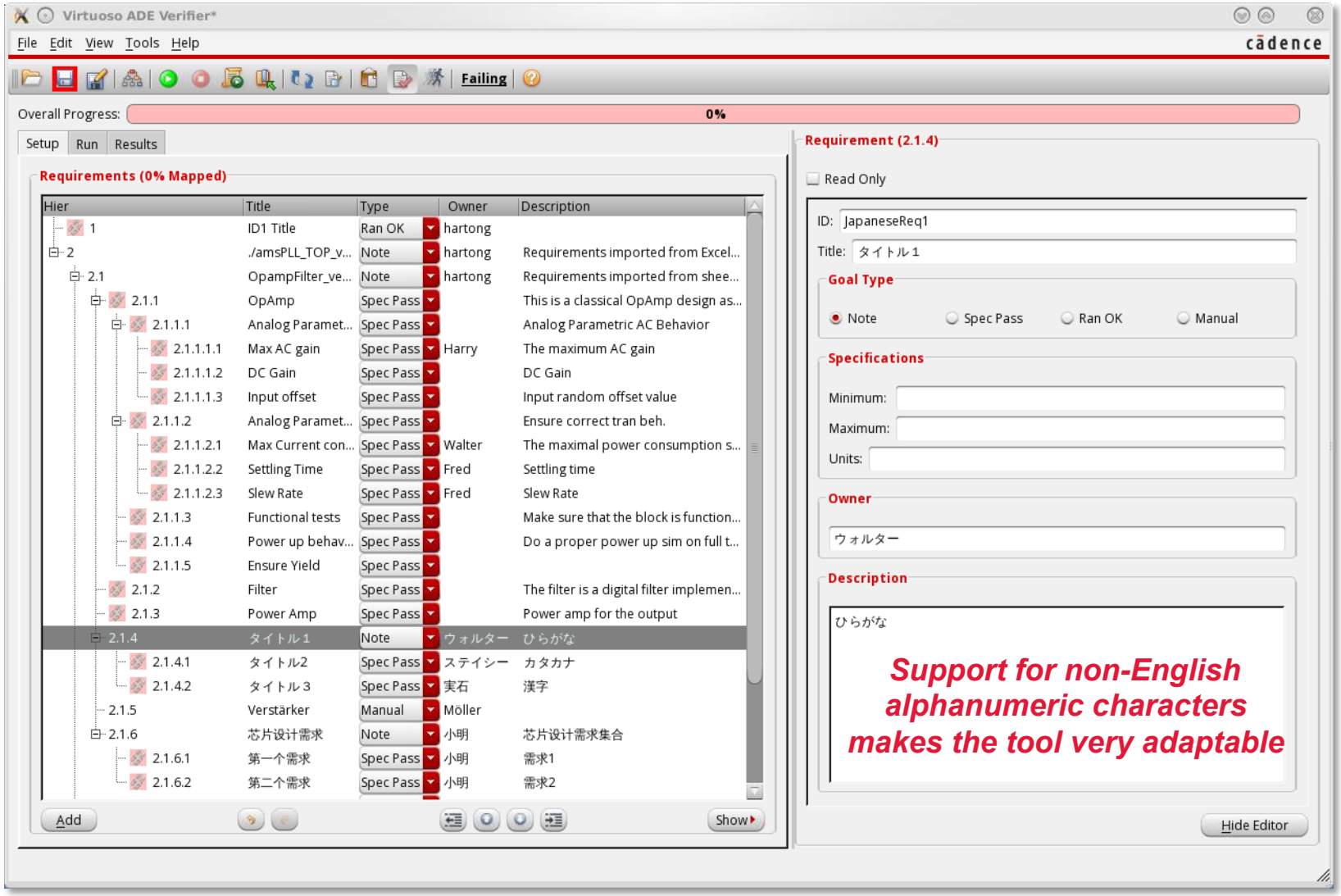
Virtuoso ADE Verifier

Support for non-English characters eases adoption of the tool



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